CLAIM AMENDMENTS

1.-7. (Cancelled)

8. (Currently Amended) A method comprising:

in response to a read operation occurring over a memory bus, amplifying data signals received directly from [[a]] the memory bus into a memory controller, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

disabling the amplification at the conclusion of the read operation ~~triggering enablement of the amplification to an edge of said at least one data strobe signal~~.

9. (Currently Amended) The method of claim 8, further comprising ~~wherein the selectively enabling the amplification comprises:~~

~~selectively~~ enabling sense amplifiers in response to the beginning of the read operation.

10. (Currently Amended) The method of claim 8, further comprising ~~wherein the selectively enabling the amplification comprises:~~

~~selectively~~ enabling the amplification in response to the beginning of the ~~predetermined~~ read operation.

11. (Previously Presented) The method of claim 8, further comprising:

synchronizing the enabling of the amplification to the edge of said at least one data strobe signal.

12. (Previously Presented) The method of claim 8, further comprising:

communicating signals associated with a double data rate memory bus over the memory bus.

13.-20. (Cancelled)

21. (Currently Amended) ~~An apparatus~~ A memory controller comprising:

amplifiers to, in response to a read operation occurring over a memory bus, amplify data signals received directly from [[a]] the memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to ~~trigger enablement of~~ disable the amplifiers at the conclusion of the read operation ~~to an edge of said at least one data strobe signal~~.

22. (Currently Amended) The ~~apparatus~~ memory controller of claim 21, wherein the ~~second circuit selectively disables the amplifiers in response to the end of a particular read operation~~ amplifiers comprise sense amplifiers.

23. (Currently Amended) The ~~apparatus~~ memory controller of claim 21, wherein the ~~predetermined operation comprises a~~ amplifiers are enabled to amplify the data signals in response to the beginning of the read operation.

24.-28. (Cancelled)

29. (Currently Amended) A computer system comprising:

a memory;

a memory bus coupled to the memory;

a processor to initiate a ~~predetermined~~ read operation ~~with the memory over~~ on the memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals; and

a memory controller coupled to the memory bus, the memory controller comprising:

amplifiers to, in response to a read operation occurring over the memory bus, amplify data signals received directly from the memory bus;

a first circuit coupled to the amplifiers to sample the amplified data signals; and

a second circuit to ~~trigger enablement of the amplifiers to an edge of said at least one data strobe signal~~ disable the amplifiers at the conclusion of the read operation.

30. (Currently Amended) The computer system of claim 29, wherein the ~~predetermined operation comprises one of a read operation and a write~~ amplifiers are enabled in response to the beginning of the read operation.

31.42. (Cancelled)